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EXAMINER	
JEFFERSON, QUOVAUNDA	

ART UNIT	PAPER NUMBER
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/566,984	CHUA ET AL.	
	Examiner	Art Unit	
	QUOVAUNDA JEFFERSON	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings were received on July 7, 2008. These drawings are accepted.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4-12, 15-17, 20, 21 and 23-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirai (US 7037767 B2).

Regarding claim 1, Hirai teaches a method of making a transistor having first and second electrodes, a semiconductive layer, and a dielectric layer; said semiconductive layer comprising a semiconductive polymer and said dielectric layer comprising an insulating polymer; characterized in that said method comprises the steps of (i) depositing on the first electrode a layer of a solution containing material for

forming the semiconductive layer and material for forming the dielectric layer; and (Note: Column 15, lines 17-23), (ii) optionally curing the layer deposited in step (i); (Note: Column 15, lines 30-36) wherein, in step (i), the solvent drying time, the temperature of the first electrode and the weight ratio of (material for forming the dielectric layer): (material for forming the semiconductive layer) in the solution are selected so that the material for forming the semiconductive layer and the material for forming the dielectric layer phase separate by self-organisation to form an interface between the material for forming the semiconductive layer and the material for forming the dielectric layer. (Note: Column 15).

Regarding claim 2, Hirai teaches all the claimed limitations including, wherein the weight ratio of (material for forming the dielectric layer): (material for forming the semiconductive layer) is in the range of from 0.5 to 2. (Note: Column 4).

Regarding claim 4, Hirai teaches the material for forming the dielectric layer is mixed with the material for forming the semiconductive layer in the solution. (Note: Column 3, lines 65- Column 4, line 2).

Regarding claim 5, Hirai teaches the material for forming the dielectric layer comprises oligomers and/or monomers for forming the insulating polymer and the material for forming the semiconductive layer comprises a semiconductive polymer and/or oligomers for forming the semiconductive polymer. (Note: Columns 4-8).

Regarding claim 6, Hirai teaches the material for forming the dielectric layer comprises an insulating polymer and the material for forming the semiconductive layer comprises a semiconductive polymer and/or oligomers for forming the semiconductive polymer. (Note: Columns 4-8).

Regarding claim 7, Hirai teaches the material for forming the semiconductive layer and the material for forming the dielectric layer comprises a diblock polymer, said polymer comprising a semiconductive block for forming the semiconductive layer and a dielectric block for forming the dielectric layer. (Note: Columns 4-8).

Regarding claim 8, Hirai teaches the material for forming the semiconductive layer comprises one or more aromatic or heteroaromatic structural units. (Note: Columns 4-8).

Regarding claim 9, Hirai teaches the one or more aromatic or heteroaromatic units independently are selected from the group consisting of fluorenedyil, phenylene, phenylene vinylene, triarylamine, thiophenediyl, thiophene, oxadiazole and benzothiadiazole. (Note: Column 11, lines 54-64).

Regarding claim 10, Hirai teaches the material for forming the dielectric layer comprises crosslinkable groups. (Note: Columns 4-8).

Regarding claim 11, Hirai teaches the material for forming the dielectric layer comprises one or more units having a low cohesive-energy density. (Note: Columns 4-8).

Regarding claim 12, Hirai teaches the one or more units having a low cohesive-energy density are selected from the group consisting of siloxane, perfluoroalkyl, perfluoroarylede ether, perfluoroalkylene ether. (Note: Columns 4-8).

Regarding claim 15, Hirai teaches the transistor is in bottom-gate configuration. (Note: Figure 6).

Regarding claim 16, Hirai teaches the material for forming the dielectric layer comprises one or more units having high affinity for the first electrode. (Note: Figure 6).

Regarding claim 17, Hirai teaches the first electrode is surface treated prior to step (i) with a material containing one or more units having high affinity for the first electrode. (Note: Figure 6).

Regarding claim 20, Hirai teaches all the claimed limitations including, wherein the transistor is a field-effect transistor. (Note: Figure 6).

Regarding claim 21 as applied to claim 1 above, Hirai teaches all the claimed limitations including wherein the transistor is a phototransistor. (Note: Figure 2).

Regarding claim 23, Hirai teaches a method of making an electronic or optoelectronic device comprising a transistor having first and second electrodes, a semiconductive layer, and a dielectric layer; said semiconductive layer comprising a semiconductive polymer and said dielectric layer comprising an insulating polymer; characterized in that said method comprises the steps of (i) depositing on the first electrode a layer of a solution containing material for forming the semiconductive layer and material for forming the dielectric layer; and (Note: Column 15, lines 17-23) (ii) optionally curing the layer deposited in step (i); (Note: Column 15, lines 30-36) wherein, in step (i), the solvent drying time, the temperature of the first electrode and the weight ratio of (material for forming the dielectric layer): (material for forming the semiconductive layer) in the solution are selected so that the material for forming the semiconductive layer and the material for forming the dielectric layer phase separate by self-organisation to form an interface between the material for forming the semiconductive layer and the material for forming the dielectric layer. (Note: Column 15)

Regarding claim 24 and 25, Hirai teaches the electronic or optoelectronic device comprises an RF tag, electronic paper, chemical sensor, logic circuit, amplifier, or driver circuit. (Note: Figure 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 13, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai (US 7037767 B2).

Regarding claim 3, Hirai teaches the solvent drying time is in the range of from 0.1 to 100s. (Note: Column 19, lines 1-5).

In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.); *In re Geisler*, 116 F.3d 1465, 1469-71,43 USPQ2d 1362, 1365-66 (Fed. Cir. 1997) (Claim reciting thickness of a protective layer as falling within a range of "50 to 100 Angstroms" considered prima facie obvious in view of prior art reference teaching that "for suitable protection, the

thickness of the protective layer should be not less than about 10 nm [i.e., 100 Angstroms]." The court stated that "by stating that suitable protection' is provided if the protective layer is about' 100 Angstroms thick, [the prior art reference] directly teaches the use of a thickness within [applicant's] claimed range.").

Similarly, a prima facie case of obviousness exists where the claimed ranges and prior art ranges do not overlap but are close enough that one skilled in the art would have expected them to have the same properties. Titanium Metals Corp. of America v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985) (Court held as proper a rejection of a claim directed to an alloy of "having 0.8% nickel, 0.3% molybdenum, up to 0.1% iron, balance titanium" as obvious over a reference disclosing alloys of 0.75% nickel, 0.25% molybdenum, balance titanium and 0.94% nickel, 0.31% molybdenum, balance titanium.). "[A] prior art reference that discloses a range encompassing a somewhat narrower claimed range is sufficient to establish a prima facie case of obviousness." *In re Peterson*, 315 F.3d 1325, 1330, 65 USPQ2d 1379, 1382-83 (Fed. Cir. 2003). >See also *In re Harris*, 409 F.3d 1339, 74 USPQ2d 1951 (Fed. Cir. 2005)(claimed alloy held obvious over prior art alloy that taught ranges of weight percentages overlapping, and in most instances completely compassing, claimed ranges; furthermore, narrower ranges taught by reference overlapped all but one range in claimed invention). However, if the reference's disclosed range is so broad as to encompass a very large number of possible distinct compositions, this might present a situation analogous to the obviousness of a species when the prior art broadly discloses a genus. Id. See also *In*

re Baird, 16 F.3d 380, 29 USPQ2d 1550 (Fed. Cir. 1994); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); MPEP § 2144.08.

Regarding claim 13, Hirai teaches the material for forming the dielectric layer has a surface tension in the range of from 15 to 35 dyn/cm. (Note: Column 4, lines 47-63).

In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.); *In re Geisler*, 116 F.3d 1465, 1469-71,43 USPQ2d 1362, 1365-66 (Fed. Cir. 1997) (Claim reciting thickness of a protective layer as falling within a range of "50 to 100 Angstroms" considered prima facie obvious in view of prior art reference teaching that "for suitable protection, the thickness of the protective layer should be not less than about 10 nm [i.e., 100 Angstroms]." The court stated that "by stating that suitable protection' is provided if the protective layer is about' 100 Angstroms thick, [the prior art reference] directly teaches the use of a thickness within [applicant's] claimed range.").

Regarding claim 18, Hirai teaches the thickness of the dielectric layer is below 400nm. (Note: Column 9, line 32-34).

In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.); *In re Geisler*, 116 F.3d 1465, 1469-71,43 USPQ2d 1362, 1365-66 (Fed. Cir. 1997) (Claim reciting thickness of a protective layer as falling within a range of "50 to 100 Angstroms" considered prima facie obvious in view of prior art reference teaching that "for suitable protection, the thickness of the protective layer should be not less than about 10 nm [i.e., 100 Angstroms]." The court stated that "by stating that suitable protection' is provided if the protective layer is about' 100 Angstroms thick, [the prior art reference] directly teaches the use of a thickness within [applicant's] claimed range.").

Regarding claim 19, Hirai teaches the thickness of the semiconductive layer is in the range of 10 nm to 300nm. (Note: Figure 5 and 6).

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an

unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardnerv. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claim 14 is rejected under 35 U.S,C. 103(a) as being unpatentable over Hirai (US 7037767 B2) in view of Veres (US 7029945 B2).

Regarding claim 14, Hirai teaches all the limitation of claim 1 in Paragraph 5 above.

Hirai does not explicity disclose wherein the transistor is in top-gate configuration.

Veres teaches a process of manufacturing an organic field effect device is provided comprising the steps of (a) depositing from a solution an organic semiconductor layer; and (b) depositing from a solution a layer of low permittivity insulating material forming at least a part of a gate insulator, such that the low

permittivity insulating material is in contact with the organic semiconductor layer, wherein the low permittivity insulating material is of relative permittivity from 1.1 to below 3.0. In addition, an organic field effect device wherein the transistor is in top-gate configuration (Note: Figures 2c and 2d)

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to combine the invention of Veras with that of Hirai for sharp interface layers.

Response to Arguments

Applicant's arguments filed July 7, 2008 have been fully considered but they are not persuasive.

With regards to the independent claims 1 and 23, Applicant traverses the rejection of these claims using the cited prior art reference of Hirai. Applicant argues two points:

(A) "… The Examiner does not address the requirement for "the weight ratio of (material for forming the dielectric layer): (material for forming the semiconductive layer) in the solution are selected so that the material for forming the semiconductive layer and the material for forming the dielectric layer phase separate by self-organization to form

an interface between the material for forming the semiconductive layer and the material for forming the dielectric layer" but merely makes reference to column 15…"

(B) "…there is no teaching or suggestion that any portion of Hirai teaches the formation of two layers as a result of a single deposition step…."

Applicant further argues that none of the other cited prior art of record teaches these limitations.

In response to argument (A), Examiner maintains the rejection of the claims using the reference of Hirai. The limitation of "wherein, in step (i)…dielectric layer" is a mental process that does not further the claim limitation because the claim does not include a method or process for selecting the solvent drying time, the temperature for the first electrode, and the weight ratio for the layers so that this material does this self-organization to form the interface. Therefore, since Hirai teaches the formation of a semiconductor layer and a dielectric layer, it would inherent that these materials would be chosen based upon certain characteristics, so that they would form two functioning layer of a transistor device.

In response to argument (B), it is noted that the features upon which applicant relies (i.e., "single deposition step" and "two materials are in the same solution") are not recited in the rejected claim(s). Although the claims are interpreted in light of the

specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Therefore, because the claim does not clearly define the semiconductor layer and the dielectric layer are made within the same single deposition step, a process that creates these layers in multiple deposition steps meets the limitations of this claim.

Therefore, the rejection of claims 1, 2, 4-12, 15-17, 20, 21, and 23-25 under 35 USC 102(e) and the rejection of all other claims under 35 USC 103(a) using the reference of Hirai is deemed proper by the Examiner.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUOVAUNDA JEFFERSON whose telephone number is (571)272-5051. The examiner can normally be reached on Monday thru Friday 7AM-3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michelle Estrada/
Primary Examiner, Art Unit 2823

QVJ